REMARKS

Anticipation Rejections

In response to the Examiner's rejection of claims 1-5, 8-11 and 14-22 under 35 U.S.C. 102(b) as being anticipated by allegedly admitted prior art, Applicant respectfully traverses the rejection because the alleged admitted prior art does not anticipate the claims and therefore the rejection is improper and should be withdrawn.

In the rejection, the examiner relies on the following passage in the background section of the specification:

> The initial MPEG decoding process typically involves de-multiplexing the different elements of the program stream (such as the audio stream, the video stream, etc.), and parsing the video, audio, sub-picture, etc. elements that are of interest. Then, the parsed elements are stored in separate buffers (video in a video buffer, audio in audio buffer,.etc.) according to their purpose for subsequent decoding. For AC-3 formatted audio data, which is most widely used in DVD playback, an error detection mechanism is employed before actual decoding begins. This error detection mechanism is the well known cyclic redundancy check (CRC) coding which detects if errors exist in the audio data. *See patent application at page 1, lines 12-19.*

While this portion of the background discloses that, for AC-3 formatted data, an error detection mechanism is used before actual decoding begins and the error detection mechanism is CRC. However, the above portion of the background (as well as no other portion of the background of the patent application) discloses each limitation of the claims as set forth below and therefore the anticipation rejection is improper.

Claims 1-9

These claims recite "enabling an error-checking hardware module upon detecting an input data packet having the predetermined format." See claim 1, for example. The background portion of the specification does not disclose a hardware error checking module. In fact, the specification specifically discloses that the known error checking is done in software. *See page*

1, lines 20-24. Thus, the specification does not disclose each feature of claim 1 and the rejection of claims 1-9 based on the allegedly admitted prior art is improper and must be withdrawn.

Claims 10 – 13

These claims recite, "checking data frames for errors; inserting an error flag into each data frame to create a flagged data frame upon detecting an error; storing each flagged data frame in a memory unit; and decoding each flagged data frame by reading the data from the memory unit and processing the flagged data frame based on the error flag" and each of these features of the claims are not shown by the alleged admitted prior art. For example, there is nothing in the background which discloses inserting an error flag into each data frame to create a flagged data frame upon detecting an error; storing each flagged data frame in a memory unit; and decoding each flagged data frame by reading the data from the memory unit and processing the flagged data frame based on the error flag. Therefore, the anticipation rejection of claims 10-13 is improper and must be withdrawn.

Claim 14

This claim recites "flagging errors in a data stream to generate a flagged data frame; and decoding a data frame by processing the flagged data frame differently from data frames that do not contain an error" and each of the these features are not disclosed by the alleged admitted prior art. Therefore, the rejection is improper and must be withdrawn.

Claims 15-23

These claims recite, in relevant part, "a hardware error-checking module that becomes enabled if the parser unit identifies a data frame having the predetermined format, wherein the error-checking module inserts an error status flag in the data frame upon finding an error; and a decoder for decoding the data stream according to the error status flag" and these elements of the claims are not disclosed by the allegedly admitted prior art. As with claim 1, the background of the specification does not disclose the hardware error checking module since the allegedly admitted prior art discloses that software is used for the error checking in typical systems. Thus, as with claim 1, the rejection of claims 15-23 is improper and must be withdrawn.

Obviousness Rejections

In response to the examiner rejection of claims 6-7, 12-13 and 23 as being unpatentable over the admitted prior art in view of US Patent No. 6,128,766 to Fahmi et al. (Fahmi), Applicant traverses the rejection because Fahmi does not cure the defect with the admitted prior art set forth above and therefore, the combination of Fahmi with the admitted prior art does not establish a prima facie case of obviousness and must be withdrawn.

CONCLUSION

In view of the above, it is respectfully submitted that Claims 1-23 are allowable over the prior art cited by the Examiner and early allowance of these claims and the application is respectfully requested.

The Examiner is invited to call Applicant's attorney at the number below in order to speed the prosecution of this application.

The Commissioner is authorized to charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 07-1896.

Respectfully submitted,

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